

An 8-bit 20-MS/s ZCBC Time-Domain Analog-to-Digital Data Converter

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Abstract—An 8-bit 20-MS/s time-domain analog-to-digital data converter (ADC) using the zero-crossing-based circuit technique is presented. Compared with the conventional ADCs, signal processing is executed in both the voltage and time domains. Since no high-gain operational amplifier is needed, this time-domain ADC works well in a low supply voltage. The proposed ADC has been fabricated in a 0.18- μm CMOS process. Its power dissipation is 4.64 mW from a supply voltage of 1.8 V. This active area occupies $1.2 \times 0.7 \text{ mm}^2$. The measured signal-to-noise-distortion ratio achieves 44.2 dB at an input frequency of 10 MHz. The integral nonlinearity is less than ± 1.07 LSB, and the differential nonlinearity is less than ± 0.72 LSB. This time-domain ADC achieves the effective bits of 7.1 for a Nyquist input frequency at 20 MS/s.

Index Terms—Analog-to-digital converter (ADC), delay-locked loop (DLL), time domain, zero-crossing-based circuit (ZCBC).

I. INTRODUCTION

TRADITIONAL analog-to-digital data converters (ADCs) have to amplify or compare a small voltage difference between the input and reference voltages in the voltage domain. Thus, the high-gain comparators or operational amplifiers (op amps) are required. For the advance CMOS process, such as 90- and 65-nm processes, the supply voltage is decreased to ensure the reliability of the devices. It is difficult to realize the high-gain and high-linearity op amp for the supply voltage lower than 1.2 V. To deal with this problem, some comparator-based switched-capacitor techniques have been reported [1]–[3]. Since the devices in the advance CMOS process have a very short delay time and a low supply voltage, it is attractive to realize the ADCs in the time domain [3] rather than in the voltage domain. Recently, a successive approximation register ADC with a time-domain comparator has been presented in [3].

In this brief, an 8-bit 20-MS/s time-domain ADC using the zero-crossing-based circuit (ZCBC) technique [2] is presented. Compared with the conventional ADCs, it releases the low-voltage limitation by the time-domain operation and is particularly well suited for operation at low supply voltages. This brief is organized as follows. Section II describes the circuit implementation. Section III shows the experimental results. Finally, the conclusions are given in Section IV.

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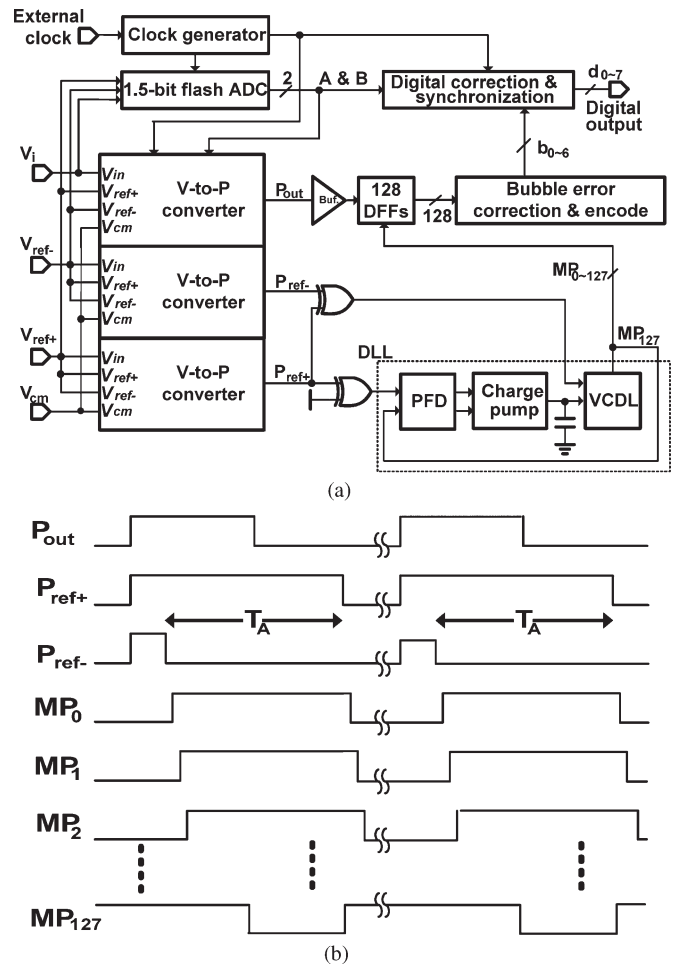


Fig. 1. (a) Time-domain ADC. (b) Timing diagram.

II. CIRCUIT DESCRIPTION

The proposed time-domain ADC and its timing diagram are shown in Fig. 1. It is composed of a clock generator, a coarse 1.5-bit Flash ADC, three voltage-to-pulsewidth converters (VPCs), a multiphase delay-locked loop (DLL), and some digital circuits.

First, the coarse comparison is performed by the 1.5-bit Flash ADC. Then, analog input and two reference voltages are converted into three pulses, i.e., P_{out} , $P_{\text{ref+}}$, and $P_{\text{ref-}}$, respectively. The pulsewidth difference T_A between $P_{\text{ref+}}$ and $P_{\text{ref-}}$, is locked with a multiphase DLL. This multiphase DLL will generate the evenly spaced multiphase clocks MP_0 – MP_{127} within the pulsewidth difference T_A . These multiphase clocks are used to sample the pulse P_{out} , which is proportional to

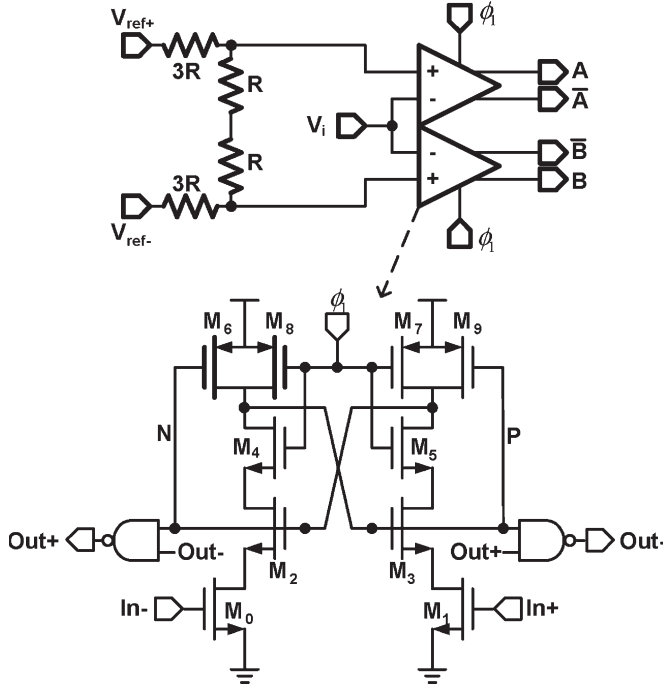


Fig. 2. Coarse 1.5-bit Flash ADC.

the input voltage. Subsequently, the bubble error correction for this 128-bit digital thermometer code is performed, and it is encoded into a 7-bit digital output. Finally, the digital error correction is used to combine the voltage-domain result of the 1.5-bit Flash ADC and the time-domain result of the 7-bit encoder. Then, the data flip-flops (DFFs) synchronize them as the final 8-bit output. The detail circuits are discussed as follows.

A. 1.5-bit Flash ADC

In an 8-bit 20-MS/s time-domain ADC without an auxiliary Flash ADC, the total required number of multiphase clocks is 256, and the pulsewidth difference T_A for a full-scale voltage is around 12 ns. The number of delay cells in a DLL will also be 256. However, under a worst-case scenario, the total intrinsic delay of these 256 delay cells in a 0.18- μm process will be larger than 12 ns. It means that these 256 delay cells cannot be locked in a DLL, and this DLL may not provide 256 multiphase clocks. To sample the pulse converted from the input voltage, there are 256 DFFs required. Moreover, 256 DFFs not only occupy a large chip area but also dissipate a lot of power. To solve the aforementioned problems, a 1.5-bit Flash ADC is adopted in this work. Therefore, a coarse Flash ADC in the voltage domain is needed.

This 1.5-bit Flash ADC is shown in Fig. 2, and it is composed of two dynamic comparators and a resistor string. The error caused by the offset voltage of the comparators is corrected by the digital error correction circuit. This Flash ADC has two operation modes: 1) reset mode and 2) amplifying mode. First, when the clock ϕ_1 is low, the comparator works in the reset mode. The transistors M_8 and M_7 preset the voltages at nodes P and N to high without changing the output results. In the amplifying mode, when ϕ_1 is high, M_4 and M_5 are turned on.

If the input voltage $In+$ is higher than $In-$, node N is pulled low through M_1 , M_3 , and M_5 . Node P is pulled high by M_6 . The cross-coupled positive feedback regenerates the results to a digital level.

B. VPC

In this brief, the VPC is realized by the ZCBC technique [2]. The VPC and its timing diagram are shown in Fig. 3. It has two nonoverlap operation phases, namely, the sampling phase ϕ_1 and the transfer phase ϕ_2 . When the sampling phase ϕ_1 is on, the input voltage is sampled on two capacitors C . The gate voltage V_x of the transistor M_1 is connected to the common voltage V_{cm} . It forces the transistors M_1 , M_2 , and M_5 to be turned on, and the output pulse P_{out} is low. The total charge in these two capacitors is

$$Q = 2C(V_{cm} - V_{in}). \quad (1)$$

After the sampling phase ϕ_1 is off, the VPC enters into the transfer phase ϕ_2 . The voltage V_y is preset to ground by a short pulse ϕ_{2a} . At this time, the voltage V_x is equal to $V_{x,init}$, and the output pulse P_{out} goes high. Then, the total charges in these two capacitors are

$$Q = C(V_{x,init} - V_{\phi_2}) + CV_{x,init} \quad (2)$$

where V_{ϕ_2} may be equal to V_{ref+} , V_{cm} , and V_{ref-} , as determined by the switches F_1 , F_2 , and F_3 , respectively. If the input voltage is higher than $0.25 V_{ref+}$, the output code AB of the Flash ADC is 00. Then, F_1 is turned on, and V_{ϕ_2} is equal to V_{ref+} . The operations of F_2 and F_3 are also similar. Substituting (2) into (1), by the charge conservation, the initial voltage of V_x in the transfer phase ϕ_2 is

$$V_{x,init} = V_{cm} - V_{in} + \frac{V_{\phi_2}}{2}. \quad (3)$$

When the voltage-domain signal is transferred to a time-domain pulse P_{out} , its pulsewidth is equal to the summation of the pulsewidth T_s of ϕ_{2a} , the charging time T_c of the current source, and the intrinsic delay time T_d from the gate voltage of M_1 to P_{out} . Therefore, the pulsewidth of P_{out} is expressed as

$$P_{W,out} = T_s + T_c + T_d. \quad (4)$$

The transistor M_1 is turned on when $V_x \geq V_{th}$, where V_{th} is the threshold voltage of M_1 . The charging time of the current source is given as

$$T_c = \frac{C}{I}(V_{th} - V_{x,init}) = \frac{C}{I}[(V_{in} - 0.5V_{\phi_2}) + (V_{th} - V_{cm})]. \quad (5)$$

Substituting (5) into (4), the pulsewidth $P_{W,out}$ of P_{out} is

$$P_{W,out} = \frac{C(2V_{in} - V_{\phi_2})}{2I} + T_{offset} \quad (6)$$

where the offset time $T_{offset} \triangleq (C(V_{th} - V_{cm})/I) + T_s + T_d$. This offset time may depend on process variations. Since the outputs of this 1.5-bit Flash ADC are folded at the decision

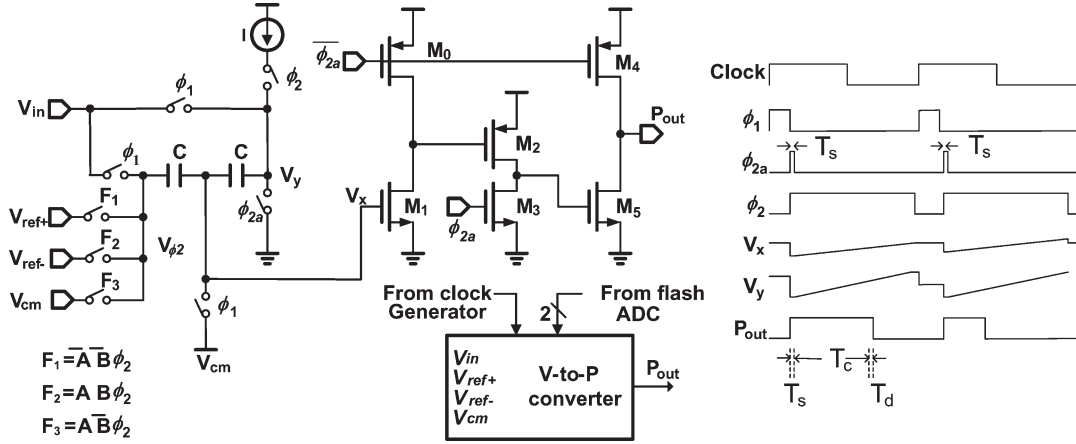


Fig. 3. Proposed VPC and its timing diagram.

points of $0.25V_{Ref\pm}$. The output of the VPC has the well-known 1.5-bit characteristic of $(2V_{in} \pm DV_{Ref})$ [4]. From (6), the output pulsewidth P_{out} also has a similar characteristic in the time domain. Thus, the digital error correction [4] can be adopted.

According to (6), the pulsewidth difference T_A is given as

$$T_A = P_{W,ref+} - P_{W,ref-} = \frac{C(V_{ref+} - V_{ref-})}{2I}. \quad (7)$$

Note that the offset time is first orderly canceled in the pulsewidth difference of (7).

The linearity of the VPCs depends on the matching of the capacitors and the current sources, which results in the differential nonlinearity (DNL), integral nonlinearity (INL), and gain error. In addition, the linearity of the current sources is subject to the channel length modulation effect, and it induces the DNL and the INL.

C. DLL

In this time-domain ADC, a multiphase clock generator is realized by using a DLL. The pulsewidth difference between P_{ref+} and P_{ref-} is locked in a DLL, and it is divided by 128 multiphase clocks. The equally spaced multiphase clocks are used to sample the output pulse P_{out} of the VPC. Usually, the voltage-controlled delay line (VCDL) with many delay cells is adopted. However, two issues should be considered. One issue is the total intrinsic delay of the delay cells. The other issue is that the phase among the delay cells is not uniformly spaced and that the nonlinearity exists. To alleviate the long intrinsic delay and the nonlinear phase space among the delay cells, the interpolation and phase averaging technique in [5] is adopted. The VCDL is shown in Fig. 4.

In Fig. 4, the VCDL has 64 cascaded delay cells, and every output has a buffer (white triangles). The auxiliary interpolation drivers (gray triangles) are inserted between two buffers for interpolation. The phase averaging resistor ring is added to improve the phase accuracy [5].

The buffers, the auxiliary interpolation driver, and the timing diagram are shown in Fig. 5. Conventionally, the clock MP_{2N+1} is interpolated from the clocks MP_{2N} and MP_{2N+2} without the auxiliary interpolation driver. When the transistors

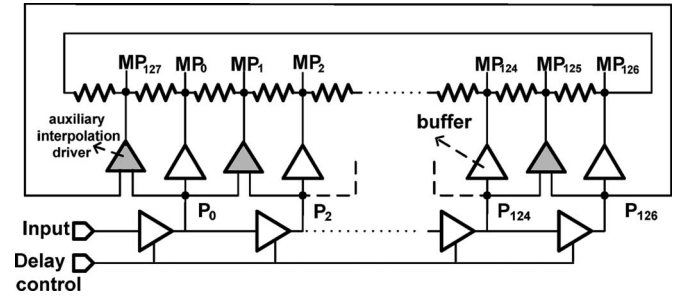


Fig. 4. VCDL in a DLL.

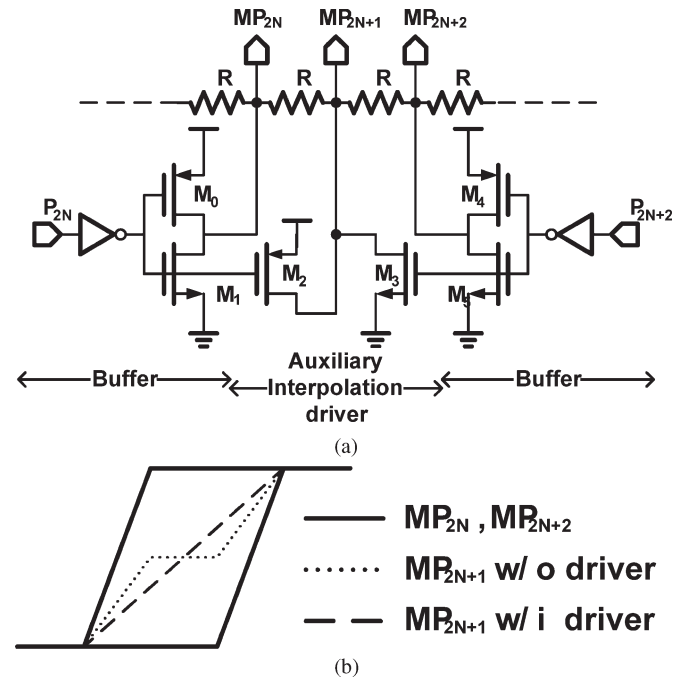


Fig. 5. (a) Buffer and auxiliary interpolation driver. (b) Transient diagram.

M_0 and M_5 are turned on to pull MP_{2N} and MP_{2N+2} to the supply voltage and ground, respectively, the clock MP_{2N+1} will be distorted severely; for example, its amplitude will stay at half of the supply for a while. In our work, the auxiliary interpolation driver is inserted on every interpolation node. The device sizes of M_2 and M_3 in this driver are much smaller than

those of M_1 and M_5 in the buffer. When MP_{2N} is rising and MP_{2N+2} is low, the NMOS M_3 is fully turned on. The drain-to-source resistance of the PMOS M_2 , i.e., R_{ds2} , is much larger than that of the NMOS M_3 . Then, the slope of MP_{2N+1} is reduced to

$$\text{Slope} \sim \frac{R_{ds3}}{R + 2R_{ds3}}. \quad (8)$$

Similarly, when MP_{2N+2} is rising and MP_{2N} is high, the slope is also reduced. Therefore, the distortion caused by the interpolation is improved so that the DLL has the multiphase clocks, which are evenly spaced.

In this DLL, the loop bandwidth of this DLL is given as

$$\text{BW} = \frac{I_{CH} K_v F_s}{C} \quad (9)$$

where I_{CH} and K_v are the charge pump current and the gain of the VCDL, which are equal to $100 \mu\text{A}$ and 6 ns/V , respectively. The loop filter C is equal to 10 pF and has a loop bandwidth of 1.2 MHz for an input clock of 20 MHz .

To convert the pulsewidth difference T_A into an M -bit code, the required number of delay cells is 2^M . The delay time t_{delay} of a delay cell is given as

$$t_{\text{delay}} < \frac{1}{2^M \cdot F_s} \quad (10)$$

where F_s is the sampling frequency. There is a speed–resolution tradeoff inherent in the generation of the clock phases in the DLL. For example, when the sampling frequency is increased from 20 to 200 MS/s , the delay time of the delay cell should also be reduced by 10 times.

D. Bubble Error Correction, Encoder, Digital Error Correction, and Synchronization

When the DLL is locked, the total delay of the VCDL is equal to the pulsewidth difference between $P_{\text{ref-}}$ and $P_{\text{ref+}}$, and there are 128 multiphase clocks, which are equally spaced in this pulsewidth difference. These clocks are applied to 128 positive-edge-trigger DFFs, which are implemented by the true single-phase clock [6] circuits, to sample the output pulse P_{out} . Since P_{out} has to drive the DFFs, a buffer is added, whose delay is close to that of an XOR gate. If the falling-edge transition time is longer than the delay time t_{delay} of delay cells, the bubble error may occur. Therefore, the three-input NAND gate array is used to correct the bubble error of the outputs of DFFs, and the falling-edge transition time is relaxed. Subsequently, one of N code-to-binary conversion is realized by an encoder. Fig. 6 shows the bubble error correction and the encoder.

Subsequently, the 1.5-bit Flash ADC requires a digital error correction circuit to produce the final digital outputs, as shown in Fig. 7. The combinational logic is implemented by two half adders, i.e.,

$$\begin{aligned} d_6 &= B \oplus t_6 \\ d_7 &= A \oplus C_{o,d_6} \end{aligned} \quad (11)$$

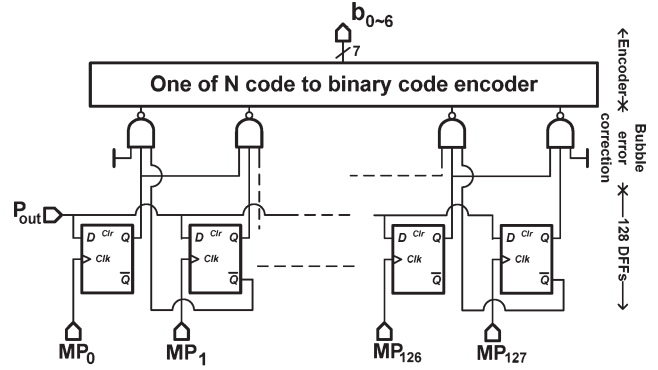


Fig. 6. DFFs, the bubble error correction, and the encoder.

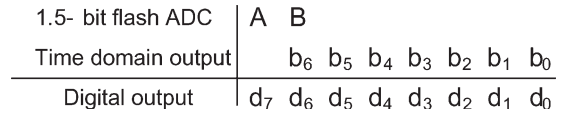


Fig. 7. Digital correction logic.

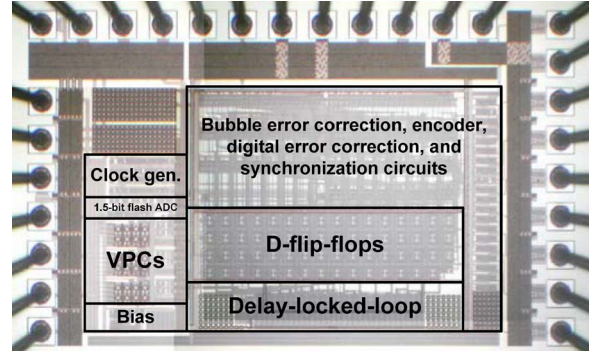


Fig. 8. Die photo.

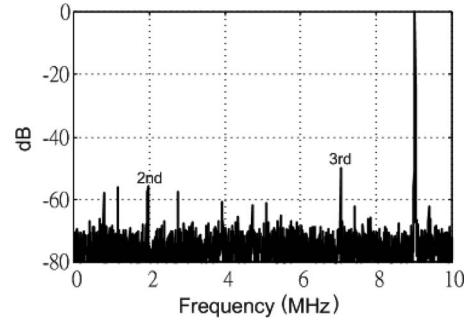


Fig. 9. Measured output spectrum.

where C_{o,d_6} is the carry bit produced while calculating d_6 . Then, the digital output is synchronized with the system clock as an 8-bit conversion result.

III. EXPERIMENTAL RESULTS

This proposed time-domain ADC has been fabricated in a $0.18\text{-}\mu\text{m}$ CMOS process. Fig. 8 shows the die photo, and its active area occupies $1.2 \times 0.7 \text{ mm}^2$. The chip is measured in the chip-on-board configuration with a supply voltage of 1.8 V . The power consumption of the ADC at 20 MS/s is 4.64 mW .

Fig. 9 shows the measured output spectrum of this proposed time-domain ADC, where the input signal is a 0.8-V_{pp}

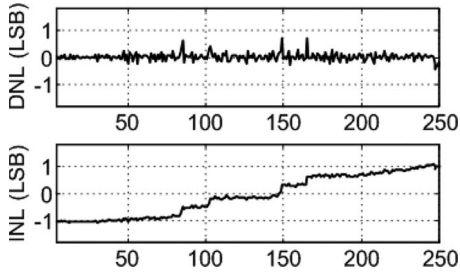


Fig. 10. Measured nonlinearity.

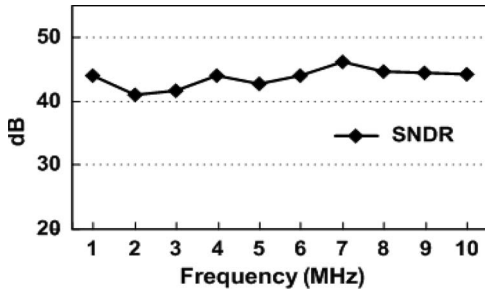


Fig. 11. Measured SNDR versus input frequency.

sinusoidal wave of 9 MHz, and this ADC is sampled at 20 MS/s. The measured spurious-free dynamic range is 50 dB, and the signal-to-noise-distortion ratio (SNDR) is 44.6 dB. The calculated effective number of bits (ENOB) is 7.1 bits.

The measured DNL and INL are shown in Fig. 10. The INL is less than ± 1.07 LSB, and the DNL is less than ± 0.72 LSB. Fig. 11 shows the measured SNDR for input frequencies from 1 MHz to 10 MHz in a step of 1 MHz at 20 MS/s. It reveals that the SNDR achieves 46.1 and 44.2 dB at input frequencies of 7 MHz and 10 MHz, respectively. Because of the absence of a sample-and-hold circuit in the input front end, there is still a small voltage difference between the inputs of VPCs and the 1.5-bit Flash ADC. In the INL plot, the systematic jumps occur at the 1.5-bit quantizer thresholds, and a 5-dB variation appears in the SNDR.

A common figure of merit (FOM) [7] is used to compare the ADC performance, which is given as

$$\text{FOM} = \frac{P_{\text{diss}}}{2^{\text{ENOB}} \times 2 \times f_{\text{BW}}} \quad (12)$$

where f_{BW} is the effective resolution bandwidth, and P_{diss} is the power consumption of the ADC. The measured performance summary and comparison are given in Table I.

IV. CONCLUSION

In this brief, an 8-bit 20-MS/s ZCBC time-domain ADC has been presented. A 1.5-bit Flash ADC was used to reduce

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Item	[2]	[8]	[9]	This work
Process	0.18 μm	0.18 μm	0.13 μm	0.18 μm
Architecture	Pipelined	SAR	SAR	Time domain
Resolution	8	8	14	8
Supply voltage	1.8V	1V	1.5V	1.8V
Sample rate	200MS/s	500KS/s	40MS/s	20MS/s
Input bandwidth	100MHz	250kHz	2.5MHz	10MHz
DNL/INL (\pm LSB)	0.75/1.0	0.24/0.31	---	0.72/1.07
SNDR	39.6dB	46.92dB	83dB	44.2dB
SFDR	---	62.69dB	---	50dB
Power	8.5mW	7.75 μW	66mW	4.64mW
Area(mm^2)	0.05	1	0.55	0.84
FOM(E/conv-step)	0.5pJ	0.09pJ	1.14pJ	1.6pJ

the intrinsic delay requirement of a VCDL and the number of DFFs. A DLL was adopted to generate multiphase clocks using the phase averaging and interpolation technique [4]. It is aimed at realizing multiphase clocks with uniform phase spacing. This time-domain ADC has been fabricated in a 0.18- μm CMOS process. The proposed ADC achieves the ENOB of 7.1 bits with the DNL and INL of ± 0.72 and ± 1.07 LSB, respectively. Because of no high-gain and high-linear op amps or comparators, it may be suitable for advanced CMOS processes.

ACKNOWLEDGMENT

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