

Efficiency-enhanced CMOS rectifier for wireless telemetry

C.-L. Chen, K.-H. Chen and S.-I. Liu

An efficiency-enhanced CMOS full-wave rectifier with low dropout voltage is presented. Both the conventional and the proposed rectifiers have been fabricated in a 0.35 μm CMOS process. Experimental results show the output voltage of the proposed rectifier is greater than that of the conventional one. Moreover, the proposed rectifier improves efficiency by more than 10%, compared with the conventional one.

Introduction: Wireless telemetry systems are widely found in medical systems, factory automation systems, air conditioning systems, security systems, etc. They can transmit and receive the data through coupled inductors or antennas. In particular, they can convert the received AC signals into a DC voltage, which serves as the power supply for wireless telemetry systems. One of the popular applications is radio frequency identification (RFID) [1]. To realise AC-to-DC conversion, the conventional full-wave rectifier is often used [2].

The conventional full-wave rectifier is composed of diode-connected PMOS and NMOS transistors as shown in Fig. 1, where V_{rf+} and V_{rf-} are differential AC signals. The PMOS transistor, M_{p1} , conducts and delivers the current, I_d to the output, when the input voltage V_{rf+} is higher than $V_{out} + V_{drop}$, where V_{drop} is the rectifier's dropout voltage. Then, the current, I_d passes through the load to the ground and returns back to V_{rf-} by the NMOS transistor M_{n2} . The rectified output voltage is expressed as

$$V_{out} = V_{rf} - V_{drop} \quad (1)$$

and the dropout voltage is

$$V_{drop} = |V_{th}| + \sqrt{\frac{2I_d}{\mu C_{ox} (W/L)}} \quad (2)$$

where μC_{ox} is the transconductance parameter, V_{th} is the threshold voltage of the PMOS transistor, M_{p1} , and W/L is its aspect ratio. Similarly, when the input voltage V_{rf-} is higher than $V_{out} + V_{drop}$, the current flows by the PMOS transistor, M_{p2} , and NMOS transistor M_{n1} . From (2), as the conduction current I_d operates in the range of mA, the dropout voltage is significantly large. It degrades the rectified output voltage and power efficiency significantly. To minimise the dropout voltage, the aspect ratio W/L should be increased. However, increasing the width of a rectifier also increases the reverse current, the parasitic capacitance, and the dissipation loss [2]. To enhance the efficiency of the rectifier, an active rectifier with low dropout voltage is presented in this Letter.

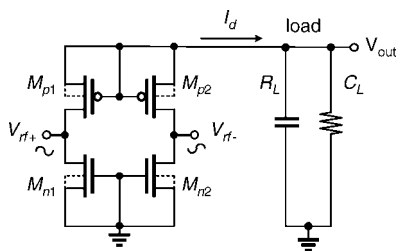


Fig. 1 Conventional full-wave rectifier

Circuit description: Fig. 2 shows the proposed rectifier with low dropout voltage. M_{p1} and M_{n1} represent the main conducting PMOS and NMOS transistors, respectively. The triode transistors M_{R1} - M_{R6} act as the resistors. M_1 - M_6 control the gate voltage of M_{p1} . The lower part of Fig. 2 is realised by the same circuits in the upper one. To reduce the dropout voltage, M_{p1} is expected to turn on completely as the input voltage $V_{rf\pm}$ is higher than the rectified voltage V_{out} , and turn off immediately as $V_{rf\pm}$ is lower than V_{out} , while preventing the reverse leakage current from V_{out} to $V_{rf\pm}$. Let M_{R4} - M_{R6} realise a large resistor. The current through M_4 is very small and the gate voltage of M_4 and M_1 is around $V_{out} - |V_{th4}|$ where $|V_{th4}|$ is the threshold voltage

of M_4 . Thus, M_1 turns on if

$$V_{rf+} > V_{out} - |V_{th4}| + |V_{th1}| \quad (3)$$

where $|V_{th1}|$ is the threshold voltage of M_1 . From (3), the dropout voltage is reduced if $|V_{th4}|$ is close to $|V_{th1}|$. As M_1 turns on, the gate voltage of M_6 is pulled high. The drain voltage of M_6 and the gate voltage of M_5 are pulled down. Meanwhile, M_2 is off. Then, M_{p1} is turned on to deliver the current from the input to the output load. Similarly, M_2 is turned on when

$$V_{out} > V_{rf+} - |V_{th3}| + |V_{th2}| \quad (4)$$

As M_2 turns on, the gate voltage of M_{p1} is immediately pulled high to prevent the reverse current from the load back to the input. From (3) and (4), the dropout voltage of the proposed rectifier is reduced and its efficiency would be significantly enhanced.

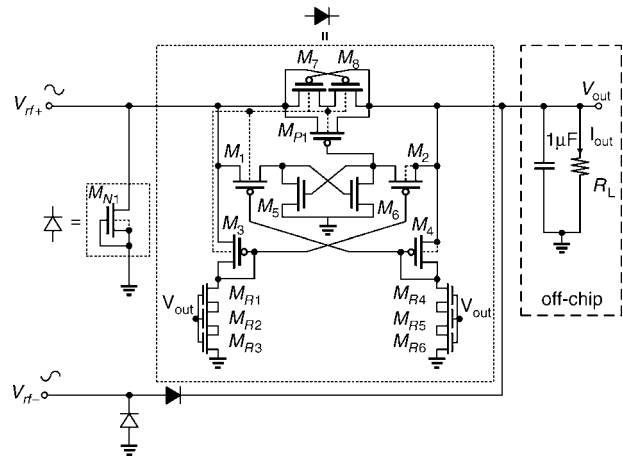


Fig. 2 Proposed full-wave rectifier with low dropout voltage

Two auxiliary PMOS transistors, M_7 and M_8 , are added to connect the substrate of M_{p1} , M_1 , M_3 , M_7 and M_8 to a higher potential. The substrate of M_{p1} , M_1 , M_3 , M_7 and M_8 is connected to V_{rf+} when V_{rf+} is higher than $V_{out} + |V_{th7}|$. When V_{rf+} is less than $V_{out} - |V_{th8}|$, the substrate of M_{p1} , M_1 , M_3 , M_7 and M_8 is connected to V_{out} . Since no current passes through these two auxiliary PMOS transistors simultaneously, their drain-source voltages are close to zero. It prevents the parasitic vertical PNP transistors from turning on and avoids the chance for latch-up [3]. Furthermore, the body effect on M_{p1} is reduced and thus also reduces the rectifier's dropout voltage and power dissipation. In addition, the cross-coupled pair, M_5 and M_6 , provides a positive feedback to generate a bistable condition which reserves a tolerance region for the unwanted noise and input coupling ripples.

Experimental results: Both the conventional rectifier in Fig. 1 and the proposed one in Fig. 2 have been fabricated in a 0.35 μm CMOS process. The die photos are shown in Fig. 3, the core area being 0.036 and 0.044 mm^2 for the conventional and the proposed rectifiers, respectively. To compare the conventional and the proposed rectifiers, the main conducting transistors for both circuits have the same size ($W = 200 \mu\text{m}$, $L = 0.5 \mu\text{m}$). Two synchronous and differential AC signals of 1 MHz are applied to the rectifiers from the signal generators with an impedance of 50 Ω via coaxial cables and coupling capacitors of 1 μF . The output voltage is measured across a 1 μF capacitor and a 2 k Ω load resistor. Fig. 4 shows the measured output voltage and efficiency against input power for the conventional and the proposed rectifiers. The efficiency is defined as $\eta = (V_{out(rms)} \times I_{out(rms)}) / (2 \times V_{rf(rms)} \times I_{rf(rms)}) \times 100\%$ where V_{out} and I_{out} are the output voltage and output current; V_{rf} and I_{rf} are the input voltage and input current, which are measured by an oscilloscope and a current probe. The denominator multiplied by two indicates that there are two differential RF signals. The measured output voltage of the proposed rectifier is greater than that of the conventional one. The measured efficiency of the proposed rectifier is higher than that of the conventional one. The maximum efficiency of the proposed rectifier is 42% at input power of 8 dBm. For the proposed rectifier, as the input power is over 8 dBm, the efficiency decreases with increasing input power. This is explained as follows. When both the conduction

current and the output voltage of the proposed rectifier are increased, the internal power dissipation of the proposed rectifier is also increased to lower the efficiency. When the output voltage is increased too much, breakdown may occur. In general, the proposed rectifier improves efficiency by more than 10%, compared with the conventional one.

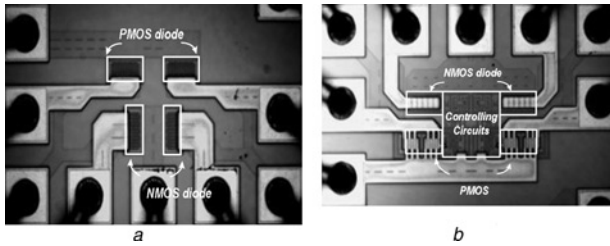


Fig. 3 Die photos of conventional and proposed rectifier

a Conventional
b Proposed

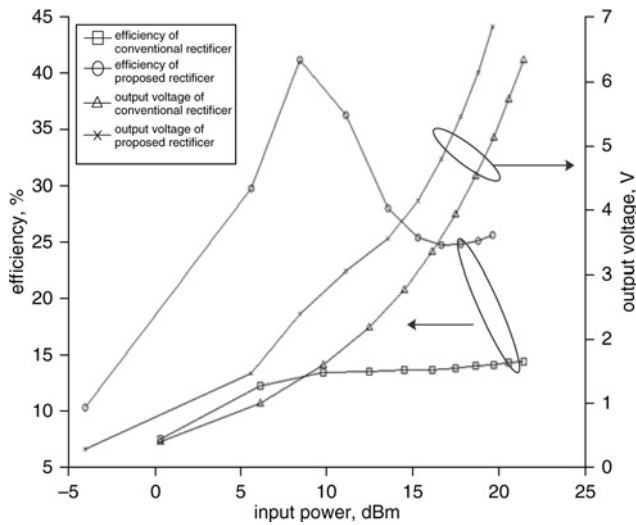


Fig. 4 Measured output and efficiency against input power for conventional and proposed rectifiers, respectively, for load of 2 k Ω

Conclusion: An active CMOS rectifier with low dropout voltage is presented. The experimental results for both the conventional rectifier and the proposed rectifier are compared. It demonstrates that both the rectified voltage and efficiency are improved for the proposed rectifier. The proposed circuit will be useful in wireless telemetry systems.

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