

Single-capacitor MOSFET-C integrator using OTRA

Wenwei Chiu, Jiann-Horng Tsay, Shen-Iuan Liu, Hen-Wai Tsao and Jiann-Jong Chen

Indexing terms: Integrating circuits, MOSFET circuits, Operational transconductance amplifiers

A highly linear MOS operational transresistance amplifier (OTRA) integrator with reduced number of capacitors and MOSFET transistors is proposed. Only one capacitor is required for an integrator to achieve cancellation of MOSFET nonlinearities. The proposed integrator is insensitive to the effects of parasitic capacitances and can be interconnected without adding any buffers. Experimental results are given to verify the theoretical analysis.

Introduction: The integrator is one of the most versatile building blocks, since it can be used in leapfrog and biquad filter realisations etc. Many methods for linearising the voltage-current relationship of MOSFETs have been proposed to construct integrators for realising fully integrated continuous-time filters [1 - 5]. To reduce the required chip area and manufacturing cost, implementation of such filters with fewer capacitors and active elements is very desirable. In this Letter, we propose a highly linear MOS OTRA integrator and compare it with the approaches of MOSFET-C integrators in [1 - 4].

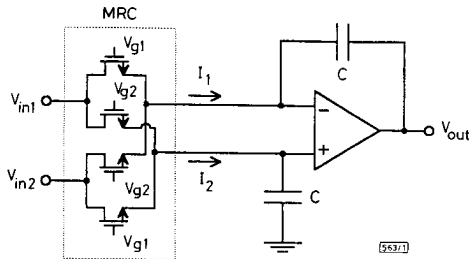


Fig. 1 Conventional MOSFET-C integrator

Integrator descriptions: The MOSFET-C integrator proposed by Czarnul *et al.* is shown in Fig. 1. This integrator can be used in a fully integrated continuous-time analogue circuit since it uses MOS transistors instead of conventional resistors. If all MOSFET transistors in the MRC block are operated in the nonsaturation region, the output of the integrator can be expressed as [1]

$$V_o = \frac{2K(V_{g2} - V_{g1})}{sC} (V_{in1} - V_{in2}) \quad (1)$$

Two capacitors are needed to construct such an integrator, which will occupy a large chip area. The mismatch between capacitors and the effect of parasitic capacitances at the input terminals of the opamp will also degrade the performance of the integrator. The second approach is an MC-based MOSFET-C integrator [2]. In this approach, only one capacitor per integrator is required, but a voltage follower must be employed as a buffer for cascading of the integrators. The parasitic capacitance at both terminals of the NIC still degrades the performance of the integrator. A third NIC-based MOSFET-C integrator is proposed by Takagi *et al.* [3]. This modified NIC-based integrator employed the half-channel width technique to reduce chip area rather than the number of MOSFETs. Only the final output stage needs to be buffered, and no voltage followers are required for interconnection of integrators. However, the parasitic capacitance is still a problem. Another approach for a MOSFET-C integrator is introduced by Brannen *et al.* [4]. The transfer characteristic of this integrator can also be written as eqn. 1. There is only one capacitor required, but it needs some additional active elements to provide bias currents. Various methods for reducing the numbers of MOSFET transistors and opamps have been discussed in [4]. Using such methods, the number of opamps can be reduced, but current sources are also required to supply bias currents. Since the input terminals of opamps are virtually grounded, the effects of parasitic capacitances can be reduced.

The MOSFET-C integrator using an OTRA is illustrated in Fig. 2. A possible method of constructing an OTRA is shown in Fig. 3. The terminal characteristics of an ideal OTRA can be described as [6]

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \quad (2)$$

For MOSFETs operating in the nonsaturation region, the difference of the two currents I_1 and I_2 can be expressed in terms of the two input voltages V_{in1} and V_{in2} as

$$I_1 - I_2 = 2K(V_{g1} - V_{g2})(V_{in1} - V_{in2}) \quad (3)$$

Consequently, if $|R_m| \rightarrow \infty$, the output voltage V_{out} can be expressed as

$$V_{out} = \frac{I_2 - I_1}{sC} = \frac{2K(V_{g2} - V_{g1})}{sC} (V_{in1} - V_{in2}) \quad (4)$$

Since the input terminals of an OTRA are virtually grounded, the proposed integrator will be insensitive to the effects of parasitic capacitances (C_{p+} and C_{p-} in Fig. 2), and the MOSFETs in MRC block, whose input terminals are connected to ground, are redundant and can be removed (because the drain and source of the MOSFETs both connect to ground). Since only one capacitor is required for this integrator, the chip area will be reduced and the problem of capacitor mismatch is eliminated.

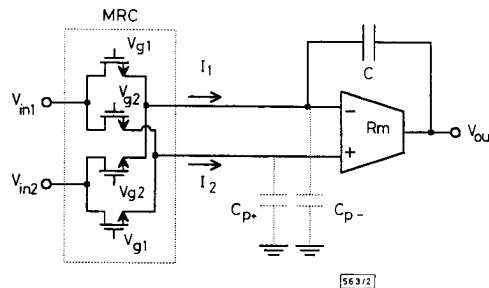


Fig. 2 Proposed integrator with some parasitic capacitances

Filter synthesis: Filters realised by the proposed integrators have a large number of redundant MOSFETs especially in the case of leapfrog simulation [7] and those redundant MOSFETs can be removed. The comparison of element counts used in various integrators is given in Table 1 for the case of an n th order ($n \geq 3$) low-pass filter. The number of MOSFETs in the integrator proposed by Takagi *et al.* [3] is more than for other integrators, but since some of the MOSFETs have a half channel width, the chip area of MRC is, therefore, not larger than for any of the other integrators listed in the Table. However, the saved chip area in MRCs is not significant, because the final stage still needs a buffer to drive the load circuits. Furthermore, filters with gain > 1 can not be synthesised with this integrator only, and the effects of parasitic capacitances still exist [3]. Among these approaches, the filters designed using the proposed integrator employ the least number of active and passive elements.

Table 1: Comparison of n th order lowpass filter realisation ($n \geq 3$)

Integrator	Number of MOSFETs	Number of active elements	Total number of capacitors	Parasitic capacitance insensitivity	Number of bias current sources	Number of buffers
Proposed	$4n + 2$	n	n	good	0	0
Czarnul [1]	$4n + 4$	n	$2n$	poor	0	0
Liu [2]	$4n + 4$	n	n	poor	0	n
Takagi [3]	$6n + 4$	n	n	poor	0	1
Brannen [4]	$5n + 3$	$n + 1$	n	good	n	0

Some MOSFETs have channel widths that are half of those of others

We have used commercial IC CD4007UBE to construct the OTRA circuit shown in Fig. 3. A third-order Chebyshev lowpass filter with a 1dB passband ripple was then breadboarded, and the measured frequency response is shown in Fig. 4.

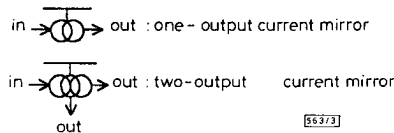
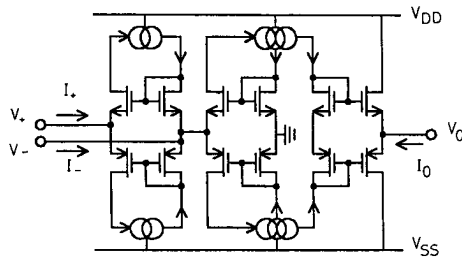


Fig. 3 OTRA circuit example

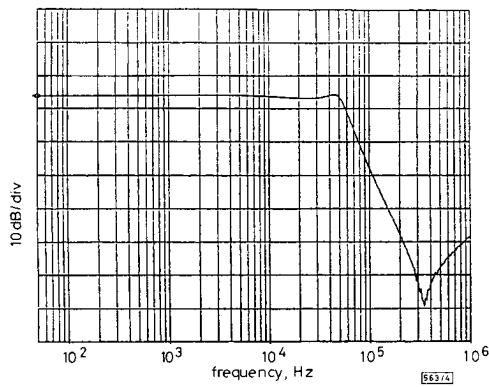


Fig. 4 Measured frequency response of third-order lowpass filter constructed using proposed integrator

Conclusion: We have described a MOSFET-C integrator using the OTRA device. The proposed integrator is insensitive to the effects of parasitic capacitances, the chip area can be reduced because only one capacitor is required and the problem of capacitor mismatch has been eliminated. A comparison of the number of elements used in various integrators has also demonstrated the superiority of the proposed integrator over other integrators. Experimental results have also been obtained to verify the theoretical analysis.

© IEE 1995

17 August 1995

Electronics Letters Online No: 19951283

Wenwei Chiu, Jiann-Horng Tsay, Shen-Iuan Liu, Hen-Wai Tsao and Jiann-Jong Chen (Department of Electrical Engineering, National Taiwan University, Taipei, 10664, Taiwan, Republic of China)

References

- 1 CZARNUL, Z.: 'Novel MOS resistive circuit for synthesis of fully integrated continuous-time filters', *IEEE Trans.*, 1986, **CAS-33**, pp. 718-721
- 2 LIU, S.-I., TSAO, H.-W., WU, J., YANG, M.-O., and TSAY, J.-H.: 'New CMOS NIC-based MOSFET-C filters', *Electron. Lett.*, 1991, **27**, pp. 772-774
- 3 TAKAGI, S., and FUJII, N.: 'Novel highly linear MOS integrator using a negative impedance converter (NIC)', *Electron. Lett.*, 1994, **30**, (10), pp. 746-748
- 4 BRANNEN, R., TAKAGI, S., ISMAIL, M., and FUJII, N.: 'New single-capacitor MOSFET-C integrators: Analysis, design and applications'. *IEEE Proc. ISCAS'94*, 1994, pp. 751-754
- 5 TAKAGI, S., FUJII, N., and YANAGISAWA, T.: 'A canonical continuous-time MOSFET-capacitor filter with high linearity'. *IEEE Proc. ISCAS'88*, 1988, pp. 2177-2180

- 6 CHEN, J.-J., TSAO, H.-W., and CHEN, C.-C.: 'Operational transresistance amplifier using CMOS technology', *Electron. Lett.*, 1992, **28**, (22), pp. 2087-2088
- 7 GIRLING, F.E.J., and GOOD, E.F.: 'Active filter: 12. The leapfrog or active-ladder synthesis', *Wirel. World*, 1970, **76**, (1417), pp. 341-345

State-space synthesis of log-domain oscillators

A. Thanachayanont, S. Pookaiyaudom and C. Toumazou

Indexing terms: Oscillators, State-space method

A state-space synthesis of oscillators based on log compression is presented. The approach is an extension of the recently proposed current-mode log domain filter synthesis methodology. Both simulated and measured results demonstrate that very low distortion oscillators can be synthesised at several megahertz using simple processing building blocks and off-the-shelf transistor arrays.

Introduction: Traditionally, oscillator circuits such as Wien Bridge, Colpitts etc., are synthesised by setting the appropriate loop gain in general operational amplifier topologies. Recently so-called 'current-mode' oscillator techniques [1] have been reported which have conventional synthesis procedures but which have potential for higher speed operation. Generally, their topologies are also well suited for IC implementation.

In this Letter, we propose a new general design methodology for high speed low distortion oscillator circuits based on the recently developed log-domain filter synthesis reported by Frey [2, 3].

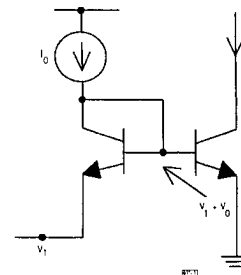


Fig. 1 Circuit for realising $I_o \exp(V_i/V_t)$

State-space synthesis of log-domain oscillator: A simple oscillator transfer function can be written as

$$T(s) = \frac{\omega_o^2}{s^2 + \omega_o^2}$$

where ω_o is the frequency of oscillation. This can be transformed to the following set of state-space equations:

$$\begin{aligned} \dot{X}_1 &= \omega_o X_2 - \omega_o X_1 \\ \dot{X}_2 &= \omega_o X_2 - 2\omega_o X_1 + \omega_o u \\ Y &= X_1 \end{aligned} \quad (1)$$

where u is the input, Y is the output and X_1 and X_2 are the state variables.

Frey showed that eqn. 1 can be transformed into a set of nodal equations by using exponential mappings on the inputs and state variables.

The following mappings are assigned to obtain the nodal equations in eqn. 2:

$$\begin{aligned} X_1 &= I_o \exp(V_1/V_t) & X_2 &= I_s \exp(V_2/V_t) \\ u &= (I_s^2/I_o) \exp(V_{01}/V_t) \end{aligned}$$